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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,236	03/26/2001	Masashi Asakawa	100021-00046	8733

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	14

DATE MAILED: 10/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,236	ASAKAWA ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama *et al.* (US Patent No. 5,574,876, hereinafter "Uchiyama") in view of Fadavi-Ardekani *et al.* (US Patent No. 6,401,176, hereinafter Fadavi-Ardekani").

3. With respect to claim 1, Uchiyama discloses a synchronous DRAM comprising:

one memory array divided into a plurality of memory blocks (Figure 1 102, see also Figure 4, MS area);

mode storage units so disposed in a plurality of stages as to correspond to said memory blocks, for storing control information for defining operation modes of said memory blocks (Figure 5A, 505 and col. 5, lines 50 – 64. MS 102 is comprised of 4 chips shown in figure 5A);

a setting unit for setting the control information designated by a mode setting instruction to said mode storage unit corresponding to said memory block designated by said mode setting instruction in accordance with said mode setting instruction outputted from a controller (col. 5, lines 60 – 64);

a mode selection unit for selecting said mode storage unit corresponding to said memory block containing a memory cell designated by an address inputted (col. 7, lines 3 – 20); and

an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of said memory blocks in accordance with the control information stored in said mode storage unit selected (This is inherent in any functional memory device, since storage of information for access is the main function of a memory device. Clock is shown in figure 6).

However, Uchiyama does not specifically disclose that mode setting instructions are outputted from a plurality of controllers. On the other hand, Fadavi-Ardekani discloses multiple controllers accessing a shared synchronous memory. It would have been obvious to one of ordinary skill in the art, having the teachings of Uchiyama and Fadavi-Ardekani before him at the time the invention was made, to use the multi-processor accessible shared synchronous memory teachings of the synchronous memory of Fadavi-Ardekani in the synchronous memory of Uchiyama, in order to allow for a more efficient use of memory resources in a multi-processor environment (Fadavi-Ardekani, col. 2, lines 35 – 43).

4. With respect to claim 2, said plurality of memory blocks is constituted by continuous memory cells designated by addresses (Uchiyama, Figure 4).

5. With respect to claim 3, wherein said plurality of memory blocks coincides with memory banks (Figures 4 and 5, memory banks 0 and 1).

6. With respect to claim 4, said setting unit includes an object selection unit for selecting said mode storage unit corresponding to a bit train on the basis of said bit train in the data outputted as a part of said mode setting instruction from a plurality of controllers, and setting it as a setting object of the control information (col. 7, lines 3 – 20, and col. 5, lines 58 – 64).

7. With respect to claim 5, said bit train is a bit train contained in the address outputted to an address bus (col. 7, lines 4 – 9).

8. With respect to claims 6, 7, and 8, wherein said bit train contained in said address is a bit train assigned to a test mode, a burst length, and CAS latency, respectively, merely recite nonfunctional description of contents of the bit train and do not patentably distinguish from their parent claim. To make them patentably distinct from the parent claims, claims should have functional utilities rather than mere assignment of labels. As currently claimed they do not claim different modes of operation of the memory. Positively claiming the different modes of operation would make them distinct from their parent claims.

9. With respect to claim 9, said bit train is a bit train contained in the data outputted to said data bus (col. 7, lines col. 10 – 13).

10. With respect to claim 10, said setting unit includes an input unit for inputting the control information to said mode storage unit as a setting object on the basis of the bit train outputted as

a part of the mode setting instruction by said plurality of controllers to said address bus (col. 7, lines 3 – 20, and col. 5, lines 58 – 64, see also figures 5 and 7).

11. With respect to claim 11, said mode selection unit includes:

a selector for acquiring information designating said memory blocks and selecting the control data outputted from the corresponding one of said mode register sets; and

an address generation unit for generating a series of addresses in accordance with the operation mode inputted (Figure 7, 704 and col. 7, lines 3 – 20).

12. With respect to claim 12, said access unit includes:

an address decoder for decoding an address input and designating the memory cell; and

an input/output control circuit for executing an access processing corresponding to the operation mode designated for the designated memory cell (figure 7, 104).

13. Rejections of claims 1 – 2 and 4 – 12 under 35 U.S.C. 103(a) based on the combined teachings of Usami and Fadavi-Ardekani detailed in the last Office Action mailed February 03, 2003, paper number 7, are maintained.

For the sake of clarity and brevity these rejection are not repeated here. Please refer to the Office Action mentioned above.

14. Rejection of claims 1 – 12 under 35 U.S.C. 103(a) based on the combined teachings of Rao and Usami detailed in the last Office Action are maintained.

15. Rejection of claims 1 – 12 under 35 U.S.C. 103(a) based on the combined teachings of Farrer and Fadavi-Ardekani detailed in the last Office Action are maintained.

Response to Arguments

16. Applicant's arguments filed July 3, 2003 have been fully considered but they are not persuasive.

17. With respect to Applicant's argument against the combined teachings of Usami and Fadavi-Ardekani, Applicant seems to be arguing that "Usami neither teaches nor suggests the features of changing the operation on one SDRAM as cited in the claim" because "Usami only discloses a control circuit that is contained in an external ASIC for setting the mode resigers." However, the independent claim as currently stated does not claim a single SDRAM unit. "A synchronous SDRAM" appearing in the preamble does not claim a single memory unit.

The recitation "A synchronous SDRAM" has not been given a full patentable weight as argued by Applicant because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See

In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In addition, "A memory" can be interpreted as a system that comprises a collection of memory cells or devices and other circuits associated with them.

18. With respect to Applicant's argument regarding Rao and Usami combination, mode setting and selection units in Rao's disclosure are identified in the rejections. Applicant has not pointed out and argued why these do not read on the claims. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

19. With respect to Farrer and Fadavi-Ardekani combination, Applicant's main argument seems to be the same as the argument against the Usami and Fadavi-Ardekani combination discussed above. Again, as currently stated the independent claim does not claim a single SDRAM device or a chip.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

whc
October 20, 2003

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100